REMARKS

The Office Action of July 17, 2006 was received and carefully reviewed. The Examiner is thanked for reviewing this application.

Claim 19-27, 80-87 and 105-123 are pending for consideration, of which claims 19, 80, 105 and 115 are independent. By this Amendment, claims 19-21, 80-82, 105-108 and 115-118 have been amended.

In the detailed Office Action, claims 19, 25, 80, 105-106, 112, and 115-116 stand rejected under 35 U.S.C. §103(a) as unpatentable over Shinya (U.S. Patent No. 5,170,158 – hereafter Shinya) in view of Lewis (U.S. Patent No. 5,589,847 – hereafter Lewis). Further, claims 26 and 113 stand rejected under 35 U.S.C. §103(a) as unpatentable over Shinya and Lewis and further in view of Friend et al. (U.S. Patent No. 5,247,190 – hereafter Friend). Still further, claims 27 and 114 stand rejected under 35 U.S.C. §103(a) as unpatentable over Shinya and Lewis and further in view of Matsueda et al. (U.S. Patent No. 6,384,806 – Matsueda). Finally, claims 86-87 and 122-123 stand rejected under 35 U.S.C. §103(a) as unpatentable over Shinya and Lewis. These rejections are respectfully traversed at least for the reasons provided below.

Initially, Applicants note that claims 86-87 and 122-123 stand rejected as unpatentable over Shinya and Lewis in further view of the same Lewis reference. As Lewis is being applied twice in the same rejection, Applicants presume this rejection is intended to be a combination of Shinya and Lewis. Applicants respectfully request the Examiner to clarify the rejection for the records.

In response to the rejections, in order to further distinguish the claimed invention over Shinya and Lewis, Applicants have amended independent claims 19, 80, 105 and 115, as shown above, to further recite a signal line driver circuit comprises a plurality of enabling circuits which limit output periods of the plurality of storage circuits. Support for the amended feature can be found at least on, e.g., page 12, lines 17-19 of the specification. In contrast with Applicants' claimed invention, Shinya and Lewis fail to teach, disclose or suggest an enabling circuit which limits output periods of a storage circuit.

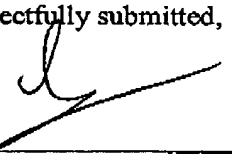
The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally

available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. As Shinya and Lewis are deficient as discussed above, the combination of Shinya and Lewis with Friends and/or Matsueda is improper.

Additionally, Applicants have amended claims 19-21, 80-82, 105-108 and 115-118, as shown above to provide proper antecedent basis for a number of limitations and to further clarify the claim language by adding "plurality" to "storage circuits" and "D/A converter circuits" where appropriate.

In view of the foregoing, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 19-27, 80-87 and 105-123 be allowed and that the application be passed to issue. If a conference would expedite prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,



Luan C. Do
Registration No. 38,434

NIXON PEABODY LLP
Suite 900, 401 9th Street, N.W.
Washington, D.C. 20004-2128
(202) 585-8000